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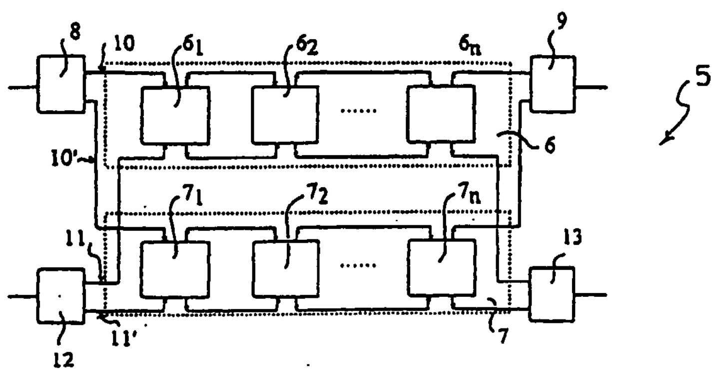

(57) Abstract

The present invention relates to an architecture for the management of transmission channels in a switch of a telecommunication system, in particular of the satellite type comprising a switching matrix connected between a plurality of input channels and a plurality of output channels. The switching matrix comprises a plurality of sub-machines (SMi), each sub-machine being connected in parallel between a sub-group of input channels for receiving a plurality of input signals (Bi) and a sub-group of output channels by means of at least one main serial transmission channel (10) of the pipeline type. The invention also relates to a structure for the transmission and channelling of digital signals connected to at least one input channel and at least one output channel, and comprising at least one chain (6) of elementary modules (6_1, 6_2,...,6_n) for the signals processing connected in cascade between each other by means of a main serial transmission channel of the pipeline type (10), each elementary module (6_1, 6_2,...,6_n) taking in input from the main serial transmission channel (10) binary information pertaining thereto and feeding in output to the main serial transmission channel (10) already processed binary information, regenerating at the same time the information carried by the main serial transmission channel (10) itself before feeding it to the next elementary module, so regenerating at the same time the entire main serial transmission channel (10) passing from one elementary module to the other.

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Title: "Architecture for managing transmission channels in telecommunication system switch, particularly for satellite applications."

DESCRIPTION

Field of application

The present invention relates to an architecture for the management of transmission channels in a switch of a telecommunication system, in particular of the satellite type.

More specifically the invention relates to an architecture for the management of transmission channels in a switch of a telecommunication system, in particular of the satellite type comprising a switching matrix connected between a plurality of input channels and a plurality of output channels.

The invention also relates to a structure for the transmission and the channelling of digital signals connected to at least one input channel and at least one output channel.

The invention relates in particular, but not exclusively, to an architecture which is able to be installed on board a satellite for telecommunications and the following description is made with reference to this field of application with the sole scope of simplifying the exposure.

Prior Art

As is well known in this specific technical field, a satellite for telecommunications can be considered as

an element of a complex transmission network. In any case, given its importance, it is usual to consider it as a telecommunication system in itself.

In general a satellite can be subdivided into :

- a first subsystem S/S BUS;
- a second subsystem S/S Payload.

The subsystem S/S BUS comprises the essential elements for the operation of the satellite, not necessarily a telecommunications satellite. It therefore comprises:

- a mechanical structure with relative mechanisms;
- a subsystem of thermic control, in order to guarantee operation in a controlled range of temperature to the electronic equipment;
- a subsystem of navigation and trim control, capable, in particular, of assuring the orientation of the satellite foreseen by the mission;
- a power subsystem capable of supplying electrical energy necessary to the carrying out of the mission to the satellite itself, in all the foreseen working conditions, protecting and isolating the loads, and delivering voltages with sufficient tolerance;
- a control and telemetry subsystem, to send commands to the satellite, control their correct execution, and know the status of the satellite itself.
- a subsystem of electronic telecommunication with the earth, also essential to each mission of whatever type (all satellites in fact, receive remote control signals and transmit telemetric signals).

In particular, such remote control signals are important in critical conditions, for example, those due to problems or failure of the satellite. In fact, it is not possible to detect the working order of the satellite directly - due to the impossibility of gaining access directly to the satellite.

In the case of a satellite for telecommunications there is also a further problem of attitude of the satellite itself, even if generally it is not necessary to regulate it so finely as in the case foreseen for satellites dedicated to astronomic missions. In fact, a variation of the attitude of the satellite and therefore of the positioning of the antenna installed on it, implies a modification of the geometry of the terrestrial cells and in a variation of the quality of the connection.

The internal configuration of the subsystem S/S Payload is instead specific for the application of the satellite itself. In the case of a satellite for telecommunications, such subsystem S/SPayload comprises the receiving RX and transmission TX sections from and for the sites on earth.

The receiving section RX is normally connected to the transmission section TX by means of a signal process chain, comprising essentially of an amplification chain, a conversion block of the input signal at a lower frequency (down-converter), a shifting block at intermediate frequency of the transmitted signal, a possible analogic switching matrix at intermediate frequency, as well as a transmission chain, complementary to the receiving chain. In this form of basic design, called non-regenerative type, the

transmission chain operates as a radio link, amplifying the signal received and re-transmitting it after having shifted it in frequency. The structure described is suitable for the transmission of signals both in analogical form and numerical form.

In the case of a numeric signal, it is possible to transform the transmission chain just mentioned by introducing a signal regeneration stage. This mode assures better quality in the signal received via satellite.

The transmission chain comprises in this case, downstream of the intermediate frequency amplifier IF, a demodulator which allows a numeric signal in base band to be obtained.

Downstream of the demodulation stage a numeric type switching matrix can be installed (commonly referred to with the term "digital switching matrix"). Even in the case of regenerative satellites, the transmission chain is complementary to that of receiving, comprising a modulator, an up-conversion chain and some amplification stages, as previously seen. In more complicated schemes, it is possible to operate with intermediate steps on the signal transmitted, for example, carrying out a de-coding/coding by means of suitable devices. In such schemes it is possible to further foresee different coding types for the signal received and for that transmitted.

Likewise it is possible to foresee intermediate operations of modification of the signal flows, in the case of connections between terminals with characteristics of the signals to or from the satellite which are different from each other. Such intermediate

elaboration operations of the flow of signals turn out to be particularly important, since the user terminals, the cost of which is a determining element in the economic feasibility of the entire system of satellite communication, represent a strong constraint in the designing of the entire telecommunication system.

Once the "bit error rate" has been fixed and the availability of connections in a certain geographical area, as well as the signal noise ratio S/N is given, whoever designs the user terminal acts on the code, on the power and on the dimensions of the antenna, with a view to reducing its costs. In this way the design of the on board equipment is also influenced, tied by the specifications of the user terminal.

It is important to underline the fact that the S/S Payload subsystem is traditionally distinct from the S/S BUS subsystem in the architecture as a whole of the satellite. This separation is indispensable also because of the fact that in general different companies, suitably specialised, produce the different components of the satellite.

Still in view of this, certain specifications are rigidly fixed in order for equipment to be mounted onto a satellite (commonly known as on board equipment), such as for example the dimensions of the space taken up, maximum power consumption, as well as the protocol of transmission inside the satellite itself, in order to allow subsystems to co-exist, which come from various companies, often distributed in a global context.

Let us come to a specific case of a satellite for telecommunications and, in particular, as an example,

to a geostationary satellite. A satellite of this type sees the earth as a series of distinct geographic areas. These areas are commonly indicated with the term "spot". The transmissions coming from each spot can be re-transmitted towards the same spot it came from or towards other spots by means of static or modifiable connections matrices. The latter are identifiable by the term "permutation matrices".

Advantageously, based on the traffic conditions such permutation matrices are re-configured so as to assign a higher number of connections to the areas with more traffic: configuration times are established in the order of a second, so as to be absolutely reasonable for an operator and to also permit complex re-configurations. These matrices can be used together with a simple transmission chain or with a transmission-regeneration chain.

The flexibility in attributing the connections is one of the principal differences between satellite transmission and terrestrial transmission.

Even with the presence of such flexibility of attribution and distribution of available connections, one is faced anyway with cases of blocking in which it is impossible to make certain connections between users even having free and unused satellite channels available. This happens because of the structure and the functionality offered by the permutation matrix.

In order to overcome this problem we proceed by transforming the satellite into a local exchange office, to which all users have direct access: all of the area covered independent from the actual geographic distribution, is considered as one portion. In order to

do this, a switching matrix is suitably installed on board the satellite, which substitutes the permutation matrix.

With the term switching matrix we mean an apparatus for switching able to manage all the incoming and outgoing channels from the satellite's telecommunication equipment. The management of channels for telecommunication are particularly carried out in an independent way from the geographic distribution of the connections, distinguishing only the input flows/channels (also called up-link) from the output flows/channels (also called down-link) for each single area, making in this way the best use of resources, that is to say of the connections available.

Exchange offices of the flows of numeric signals for telecommunication networks have been known for some time in the field of terrestrial communications. It is just a question of equipment which is able to operate on signals, the unit of information of which is equal to 8 bits and with a capacity in the order of 100,000 channels, in the case of large stations. It can be observed that the aforementioned units of information are organised, in the various numeric data transporting circuits, in structures denominated frames, in which each unit of information occupies a very precise time position. The frames follow each other periodically in time so that the units of information follow each other with the same period of timing. Each communication (or circuit), is composed of a sequence of informative units, and therefore unmistakably identifiable just from its own time position inside the frame. Just as an example the PCM European system can be cited, in which 32 units of information of 8 bits each follow each

other to form a frame of 256 bits.

Terrestrial switching is a discipline characterised by a vast industrial involvement, dynamic - because it is based on the availability of electronic and similar technologies - historically identified with the development of "large projects" and in consequence the dominion of the large companies in the field. Local terrestrial stations can be taken as a possible reference, in that the direct connection of the users to the satellite would render the satellite functionally levelled down to a local station (or a station for cellular telephony, except for the larger band switched).

In the case of technologies for space, we find ourselves with the problem of managing a high number of channels (in the order of 500,000 per satellite). The typical problems of space applications can be added to this increase in the number of channels involved, such as the problem of the weight and power consumption of the equipment suitable for being mounted "on board", which heavily limit the possibility of installing effective redundancy structures in the equipment itself.

A further difficulty arises from the availability of the electronic components, limited to that suitable for tolerating the levels of radiation present in space.

In order to design a switching matrix capable of operating on a multitude of informative flows as previously described, which arrive separated on different inputs, it is necessary to carry out two types of operation: a time slot exchange, able to move inside a frame each single informative unit in each

possible position; and a space switching , which allows each single informative unit to reach the desired output.

The resulting switching system must have at least one space stage S, assisted by two time stages T, in order to create all possible connections between each single input and output circuit. In particular, so-called TST switches are known (or switches equivalent to STS), comprising one or more stages of input T, one or more stages of output T and a single stage S.

In order to explain the operation of a switch of the TST type, let us consider a simple transferral of information from an input line IN1 to an output line OUT2 with its simultaneous time shifting from the time position T1 to position T2. It is possible to see a case where, in order to avoid collisions inside the matrix of the stage S, it is necessary to make the time shifting in two successive steps.

In particular, an input stage T moves the information temporally into an intermediate position, or into a service position, Tm, algorithmically determined in such a way as to avoid collisions; a further output stage T therefore moves the information, transferred onto the output channel determined thanks to the stage S, into the desired final time position T2.

The two stages T create the time switchings requested, guaranteeing the complete use of the space matrix S placed between them, independent of whatever the time positions T1 and T2 may be and independent from whatever the input line IN1 and the output line OUT2 may be.

It is also advisable to specify that the complexity of the calculation of such an intermediate position Tm increases in a superlinear way with the dimensions of the matrix.

For the application in consideration the driving of this type of equipment is complex, above all from the computational point of view, having to keep account of the integrity of the information and to avoid collisions between them. Furthermore, in the case of a failure, the basic algorithm of this calculation must be parametrised.

The few known satellite switches revolve around a concept of switch developed within the European Space Agency (ESA), having a capacity of the base module, equal to 260 Mb/s, up to 2Gb/s.

The main limits of such architecture are tied to its "terrestrial" derivation, of which:

- maximum extension applicable is equal to 2 Gb/s against needs of switching of 10 Gb/s required by the satellites being designed today;

- low reconfigurability in the case of failure;

- complex control (something which transfers both into costs and development risks, as well as in the increase of mass and power consumption of the control equipment on board the satellite);

- relevant mass and absorbed power; and

- in particular, the TST solution presents the drawback of a switching delay more than double the duration of the frame.

The switch thus obtained presents therefore numerous disadvantages.

For these reasons, such switch is scarcely suited to the applications for satellite transmissions above 2 Gb/s.

The technical problem which is the basis of the present invention is to design a switch suitable for satellite applications, having structural and operational characteristics such as to allow for the management of a very high number of channels, at the same time limiting its weight and dissipated power, therefore overcoming the limitations of the solutions which make reference to switches for terrestrial stations according to prior art.

Summary of the invention

The idea of solution at the basis of this invention is to use a modular architecture based on a parallelisation of the switching matrix in order to reduce dimensions and control complexity thereof.

Furthermore, the present invention foresees the use of a serial transmission channel, able to carry both original and processed information inside the modular architecture, regenerating it in the process.

Advantageously according to the invention, the reliability of modular architecture is further guaranteed by the use of a redundancy structure for this serial transmission channel, capable of facing situations of malfunction or failure of the main channel.

On the basis of such an idea for a solution, the

technical problem is resolved by an architecture for the management of transmission channels in a switch of a system of telecommunication, in particular of the satellite type, of the type previously indicated and defined by the characterising part of claim 1.

The technical problem is further resolved by a structure for the transmission and channelling of digital signals of the type previously indicated and defined by the characterising part of claim 15.

The characteristics and advantages of the architecture for the management of transmission channels and the structure for the transmission and channelling of digital signals according to the invention will result from the description hereinbelow, of an example of embodiment given as an indication and not a limitation thereto, with reference to the attached drawings.

Brief description of the drawings

In such drawings:

- Figure 1A shows in a case taken as a mere example, a switch with n lines of input and as many lines in output, with n=256 and a frame structure composed of various informative units, so-called Frame Unit (FU).

- Figure 1 B shows a schematic view of a structure of informative units (FU):

- Figure 2 shows a schematic view of an embodiment for switching the structure of informative units of figure 1B;

- Figure 3 shows a schematic view of an architecture of "byte sliced" type according to the invention;

- Figure 4 shows a schematic view of a substitution of data of the type denominated ping-pong used in the architecture of figure 3;

- Figures 5 and 6 show respective schematic views of an example of movement of information performed by means of a pipeline according to the invention.

- Figure 7 shows as an example the possible aspect of a physical embodiment of the invention.

Detailed description

With reference to such figures an architecture for the management of transmission channels in a satellite switch will now be described.

A satellite switch according to the invention comprises essentially of a matrix, denominated herein as switching matrix, connected between a plurality of lines, or channels, of input and a plurality of lines or channels of output. Such switching matrix carries out the transferral of information present on an input channel on a suitably selected output channel, at the same carrying out a time shifting.

The information arrives at the input channels in the form of bit frames, subdivided on said plurality of input lines and suitably indexed according to the instant of receiving.

With reference to such figures, with 1 a structure of informative units is globally and schematically indicated for a switch according to the invention.

Such structure of informative units can be identical to that of input/output or be the fruit of a suitable

process, deterministically reconstructable with reference to a Frame Start Signal SIT.

A memory matrix, or sub-machine, SM1,...,SM64 is associated to each group of bit B1,...,B64.

By means of a frame structure 1 it is possible to develop a common memory switch, functionally corresponding to an STS type switch.

The advantages offered by a common memory architecture include a reduced delay in transit of the data inside the switch, the possibility of increasing the reliability with controlled increases of the dimension of the common memory, and the limited complexity of control of the memory itself and of the switch in its whole.

For space applications, the common memory, also called switching matrix given its central function in the operations of switching of the channels of input and output of the transmission system, requires furthermore the availability of memory banks, capable of being written and read at a speed of 10 Gb/s, and if necessary higher.

In practice an architecture with common memory is impossible to be designed with the techniques available at present, requiring a single integrated component as switching matrix, something which is not practically possible with the dimensions in consideration. In other words, at the present time it is not possible to design an integrated switching matrix with the magnitude order of such great numbers of channels and transmission speeds and switching required by satellite transmission.

Advantageously, the satellite switch according to the present invention parallelises the functions of switching. In particular, in a preferred design example the memory slot structure already present in known equipment is made use of, which is equal to 64 Bytes against 1 Byte of the terrestrial applications.

In fact this means thinking about the switching matrix as a plurality of memory matrices or parallel sub-machines SM1,...,SM64, each one dedicated to the processing of a byte, B1,...,B64. Advantageously according to the invention, each sub-machine SM1,...,SM64 contains a time segment of all the lines of input connected to the switch.

More in particular, in the example of embodiment herein described purely indicatively and not limiting the invention, sixty-four parallel sub-machines SM1,...,SM64, are used, which work at a peak speed of 10 Gb/s, but at an average speed equal to 1/64 of 10 Gb/s and are therefore possible even with the components already known for present applications.

Figure 1A shows, in a case given as a mere example, a switch with n lines of input and as many lines in output, with n=256 and a frame structure composed of various informative units, so-called Frame Unit (FU).

It can immediately be established that such decomposition in a plurality of parallel sub-machines avoids the necessity for programmable S stages, the main source of problems for the solutions of the prior art.

Figure 1B schematically shows also this decomposition in parallel sub-machines, indicated with the acronym

SM, "Shared Memory".

The frame structure 1 of figure 1B is implemented by means of a structure of elementary modules 2, in particular processing blocks, connected in parallel to each other between a bus 3 of input and a bus 4 of output, as illustrated in figure 2. The structure of each single module will be illustrated in detail at a later point.

By designing programmable elementary modules 2, that is modules capable of processing any portion of a slot of 64 bytes, the embodiment of the structure of frame 1 schematically illustrated in figure 2 presents also the possibility of overcoming the failure of an elementary module 2. By foreseeing a number of elementary modules 2 above the number of sub-machines SM1,....,SM64, necessary for the frame decomposition according to the invention, in this particular example equal to sixty-four, it is possible to face more failures, until the requisites for reliability required by each specific application are satisfied.

More in general, an architecture of frame structure 1 of the type illustrated in figure 1B is called "byte sliced" and is usable, without having to use further stages of switching, until the following relationship is observed:

$$C<=n/T$$

where:

C is the total capacity to be switched (normally expressed in bits/s);

n is the number of bits composing an Informative Unit;

and

T is the access time to the memory banks of the sub-machines SM1,...,SM64 selected;

The structure of frame 1 as described might present certain problems if applied directly to actual equipment for telecommunication operating on board satellite.

In fact, the structure of frame 1 comprises a single input bus on which all the information relative to the frame to be transmitted are stored.

In case of failure on the interfaces it is possible to lose at least a portion of the input bus. The switching matrix can in this case continue to operate, but at reduced capacity, that is without being able to guarantee the operation on all input and output lines.

In order to improve the reliability of the switching matrix in its whole, it is possible to think about doubling the input bus. This solution is not compatible though with the physical capacity of the connectors qualified for space applications.

Furthermore the bus, as illustrated for the embodiment in figure 2, is of the passive type, so as to avoid a multiplexer in output, the complexity of which would eliminate the advantages of the architecture of the byte sliced type according to the invention. A passive bus, moreover, is not capable of guaranteeing the stable operation of the actual switching matrix, in the conditions of speed specified (40 Mb/s in this specific example).

This requirement for "stability" of the switching

matrix is fundamental in the case of space applications, where it is necessary to guarantee the correct operation of instrumentation for missions in the order of fifteen years.

The problems tied to the reliability and stability of the structure of switching designed starting from a byte sliced architecture according to the invention have been resolved by using a single input/output bus rather than two separate buses for input and output, 3, and 4, as illustrated in figure 2.

In order to allow for the sharing of the bus of the numeric flows of input and output, the technique denominated "pipeline" is used, which transforms the passive bi-directional bus into an active and mono-directional bus. This allows an increase in the speed of transmission on the bus, with respect to systems with a passive bus of common adoption in the electronic systems with multiple boards. In this way the form of design of a byte sliced architecture 5 is obtained as illustrated in figure 3.

The byte sliced architecture 5 comprises of at least one chain 6 of elementary modules 6_1, $6_2, \ldots, 6_n$, connected to an input demultiplexer 8 and to an output multiplexer 9, via a main pipeline transmission channel 10.

Such main pipeline 10 further connects each elementary module to each other 6_1, $6_2, \ldots, 6_n$ of said chain 6.

By using a single serial pipeline 10, each elementary module extracts its own byte in input and feeds an already processed byte in output, at the same time regenerating the information transported by the

pipeline itself before feeding it to the next elementary module.

This approach therefore allows the regeneration of the entire pipeline 10 passing from one elementary module to another and, at the same time, halving the number of connections necessary.

It is necessary to point out the fact that a critical element in the implementation of the pipeline structure in figure 3 is the time relationship between the information transported by the pipeline in input and output from each elementary module. In fact during the transit of information from one module to another sequences are formed with input, that is not yet processed, bytes belonging to :

"FU input K; Frame Fi"

and output bytes, i.e. already processed by the current module or by previous ones, belonging to :

"FU output h; Frame Fj"

with h>k

and j>i

In the byte sliced architecture 5 according to the invention only at the output of the last module is the sequence of byte coherent, in that the bytes of the same informative unit FU are consecutive, without bytes belonging to other informative units of output or input being interposed between them.

In order to be clearer an example is described, in which the frame is limited to frames composed of four

informative units. Each informative unit FU is composed of four bytes. A reduced frame is used as an example to facilitate the understanding of the mechanism of operation of the byte sliced architecture 5 according to the invention, avoiding the numeric complications of an example corresponding to the actual needs of space applications.

Examining for example a particular case in which h=k+2 and j=i+1, the first module 6_1 of the chain 6 extracts the first byte of each "Fu input k+2, F i+1, and substitutes it with the first byte destined for "FU output K" and coming from "Fi", as illustrated in figure 5.

At the output of the last module 6_n, the fourth in this example, the pipeline is correctly formed and temporally shifted of one frame plus two informative units FU, as illustrated in figure 6.

The so-called "interleaving" form, in which information already processed and directed towards the output is put between information still to be processed coming from the input, which arises at each regeneration of the pipeline in an elementary module, is deterministic, and therefore allows the complete reconstruction of the correct flow of information of output.

In particular, by operating each module SM in an identical way as all the others, that is operating the substitution on the pipeline of the groups of bit extracted with those processed and pertinent to the preceding FU, according to the invention the structure of the frame at the output of the pipeline is advantageously already the one desired, without it therefore being necessary to make any further

elaboration.

In applications for space, the reduction of the number of electronic circuits is crucial for the minimisation of power consumption.

Nevertheless, for a switch of actual dimensions, the number of connections is still very high and therefore not easily compatible with the technologies of connection qualified for space.

A further optimization is therefore obtained by working on the main pipeline 10, also known as traffic pipeline, in particular by subdividing the switch into "M" sections - with "M" submultiple of "n" (number of bits composing the informative units FU).

Each section Sm (each one composed of operating modules in accordance with the above mentioned concept of byte sliced structure), processes the position bits "m + M", "m + 2M", etc.

It is important to underline the fact that such subdivision into sections maintains the time non-overlapping, in order to avoid the necessity to introduce a stage S, with the problems it gives, already seen in relation to the prior art.

The number of input/output connections per module is therefore divided by "M".

In the example in figure 3, the M=2 case has been considered, that is to say a switch divided into two sections, in particular one dedicated to the elaboration of even bits and one dedicated to odd bits.

The final architecture 5 of the byte sliced type

comprises in fact a first chain 6 and a second chain 7 of elementary modules, 6_1, 6_2,...,6_n and 7_1, 7_2,...,7_n respectively, dedicated to the parallel processing of odd and even bits respectively.

Such first and second chain of elementary modules are connected to a input demultiplexer 8 and to an output multiplexer 9, via a main pipeline 10, which connects each elementary module to each other, both of the first and of the second chain.

The input demultiplexer 8 provides for the generation of two pipelines 10 and 10', odd and even, and the output multiplexer 9 recomposes the flow of information of frame.

Advantageously according to the invention, the reliability of the machine is further guaranteed by the use of a redundancy structure by means of a pipeline of redundancy 11, identical to the main pipeline 10.

Respecting the symmetry of configuration of byte sliced architecture 5, even the pipeline of redundancy 11 is connected to a redundant input demultiplexer 12 and to a redundant output multiplexer 13. Such a redundancy structure also allows the duplication of functions of multiplexing and demultiplexing, allowing for the recovery of any failure.

Once again, the concept at the basis of this invention is preserved, each module, independent of the chain it belongs to (odd or even, in a specific example of embodiment), contains a time portion of all the channels.

The flow of traffic as a whole can travel on portions

of both the pipelines, main and of redundancy, allowing for a single failure on the interface to be adjusted: in the case of a failure it is sufficient to switch the transmission of the main pipeline to the pipeline of redundancy. According to their position even more than one failure can be adjusted.

Advantageously according to the invention, the switching of each group of data is carried out, in each module denominated SM, by means of a double memory bank which operates in successive frame ranges alternating the functions carried out by each single bank, in a so-called "ping-pong" way, as schematically illustrated in figure 4.

Each elementary module therefore comprises an input controller 14 connected to an output controller 15 via a first memory bank 16 and a second memory bank 17, operating in alternate cycles, of a duration equal to the duration of an entire frame. For example, in one cycle the memory bank 16 stores the data coming from the input controller 14, whilst the memory bank 17 sends the data stored in the previous cycle to the output controller 15. In the next cycle the two banks exchange the repetitive functions, so that the memory bank 17 stores the data coming from the input controller 14, whilst the memory bank 16 sends the data stored in the previous cycle to the output controller 15.

Furthermore, the byte sliced architecture 5 according to the invention advantageously carries out a demultiplexing (and following multiplexing) bit to bit (instead of, for example, byte to byte), minimising in this way the number of registers necessary for carrying

out such operation and therefore the power consumption, a parameter which is always critical in applications for space.

Furthermore, the use of a main pipeline and a pipeline of redundancy allows the number of the connections necessary for the final switch to be reduced.

It is possible to further improve the performances of the switch obtained by operating a subdivision of the pipeline relative to a connection memory DM (Driving Memory).

In particular, the connection memory DM contains the order of the re-reading of the data previously stored in each module SM in sequential order. The suitable order of re-reading of the data allows each byte to be inserted in a suitable position on the pipeline in such a way that at the output it will be placed in the suitable output line in a suitable time position.

When the speed of writing of the sub-machines is lower than the maximum speed used in the switching matrix, it is possible to time multiplex the addresses of the memory, further reducing the number of connections, as long as the relative speeds are in whole ratio amongst each other, as always possible according to the present invention.

In the referred case, for example, the traffic pipeline operates at a speed of 40 Mb/s whilst the sub-machines operate at 20 Mb/s with an address bus having 19 lines (for a total of 524,288 addresses).Multiplexing the addresses of memory at 40 Mb/s it is possible to also reduce to about a half the lines of the pipeline of the memory of connection, which can therefore use 10 lines

instead of 19 lines.

In order to minimise the number of registers, the various sub-machines carry out the reading in parallel of the bytes of their competence, or use the current memory address present on the pipeline.

In principle each sub-machine SM could receive and regenerate all the flow of information transported in the switching matrix, providing, in the specific example, a cascade of thirty-two sub-machines per switching matrix.

In practice, more sub-machine Sms are grouped on the same physical board. This means a simplification of the switching matrix in its whole.

The sub-machines SM grouped on the same board are in fact connected via a passive bus, not adopted as far as the whole switching matrix is concerned, because of the problems it causes.

As far as the board is concerned, the reduced number of sub-machines SM (and therefore the related problems of fan-out), and the reduced distances (and therefore easier synchronisation), makes possible the adoption of the passive bus, for example, by means of a similar and reduced structure of the embodiment in figure 2.

There are still critical problems, tied to the transition of the passive bus of the sub-machine, which occur when a sub-machine Smi stops to transmit data onto the passive bus. Both the sub-machines Smi and Smj use signal amplifiers of the "tristate" type in the interfaces towards the passive bus, that is to say amplification elements with the capacity to put

themselves in a state of high impedance (the so-called "tristate") which allows other similar elements to use the passive bus. So designed "tristate" elements present an equivalent output capacity needing suitable discharge times, in particular equal to about 10 ns, with present technologies. In this period of transition the information sent onto the passive bus is not reliable. In the worst case each single sub-machine SM operates by transmitting only one byte onto the bus, so a transition for each byte transmitted could possibly occur.

This difficulty is resolved by making the sub-machines of the same board work on alternate bytes, therefore avoiding two sub-machines accessing the output bus consecutively: this is called "interlacing of the bytes".

In this way, advantageously according to the invention, operating on bytes which are not temporally adjacent, means it is possible to have dead periods essential for the passive bus which uses tristate elements.

Since each sub-machine is programmable by remote control, it is possible to connect to the passive bus more sub-machines than are necessary.

That is, being "p" the design number of such sub-machines at a lower level, advantageously it is possible to connect "q" sub-machines at a lower level, with q>p, in order to guard against possible failures through the remote control, increasing in this way the reliability of the single elementary module connected to the serial bus.

A unit of switching designed in accordance with the

present invention in assembled form, would take the aspect shown as an example in figure 7.

In conclusion, the satellite switch according to the invention presents four specific technical elements:

- a new process structure of byte sliced type;

- a resolution of the synchronisms and of the redundancy based on the use of a double pipeline, main and of redundancy, denominated "dual bus with detour";

- a resolution of the connections by means of the multiplexing of data bit to bit and the use of a connection memory, driving memory DM, equipped with a pipeline with "dual bus detour" type structure;

- a robustness of the intermodular bus by means of the so-called interlacing of the bytes.

CLAIMS

1. Architecture for the management of transmission channels in a switch of a system of telecommunication, in particular of the satellite type comprising a switching matrix connected between a plurality of input channels and a plurality of output channels, characterised in that, said switching matrix comprises a plurality of sub-machines (SMi), each sub-machine being connected in parallel between a sub-group of said input channels for receiving a plurality of input signals (Bi) and a sub-group of said output channels by means of at least one main serial transmission channel of the pipeline (10) type.

2. Architecture for the management of transmission channels according to claim 1, characterised in that it further comprises a serial transmission channel of redundancy (11), also fed by said plurality of input signals (Bi) in such a way as to be able to face situations of malfunction or failure of the main channel of serial transmission (10).

3. Architecture for the management of transmission channels according to claim 1, characterised in that it comprises at least one transmission chain (6) of elementary modules or sets of elementary modules (6_1, 6_2,...,6_n) for the processing of signals, each of which corresponds to a sub-machine of said plurality of sub-machines (SMi), said elementary modules (6_1, 6_2,...,6_n) for the processing of signals being connected in cascade between each other by means of said main channel of serial transmission (10).

4. Architecture for the management of transmission

channels according to claim 3, characterised in that said transmission chain (6) of elementary modules or sets of elementary modules (6_1, $6_2, \ldots, 6_n$) for the processing of signals is connected by means of said main channel of serial transmission (10), to an input demultiplexer (8), which is connected in input to said sub-group of input channels, and to an output multiplexer (9), which is connected in output to said sub-group of output channels.

5. Architecture for the management of transmission channels according to claim 4, characterised in that each elementary module or set of elementary modules (6_1, $6_2, \ldots, 6_n$) for the signals processing gets in input from the main channel of serial transmission (10) binary information pertaining thereto and supplies in output to the main channel of serial transmission (10) binary information already processed, at the same time regenerating the information carried by the main channel of serial transmission (10) itself before feeding it to the next elementary module, so regenerating the entire main channel of serial transmission (10) passing from one elementary module to the other.

6. Architecture for the management of transmission channels according to claims 2 and 3, characterised in that said elementary modules or set of elementary modules (6_1, $6_2, \ldots, 6_n$) for the signals processing are further connected in cascade between each other by means of said serial transmission channel of redundancy (11).

7. Architecture for the management of transmission channels according to claims 4 and 6, characterised in

that said transmission chain (6) of elementary modules or sets of elementary modules (6_1, 6_2,...,6_n) for the signals processing is connected, by means of said serial transmission channel of redundancy(11), to an input demultiplexer of redundancy (12), which is connected in input to a further sub-group of input channels, and to an output multiplexer of redundancy (13), which is connected in output to a further sub-group of output channels.

8. Architecture for the management of transmission channels according to claim 7, characterised in that it further comprises a second transmission chain (7) of elementary modules or sets of elementary modules (7_1, 7_2,...,7_n) for the signals processing connected in cascade between each other by means of said main channel of serial transmission (10) and by means of said serial transmission channel of redundancy(11), and also to said input demultiplexers (8, 12) and said output multiplexers (9, 12).

9. Architecture for the management of transmission channels according to claim 3, characterised in that it foresees further elementary modules for the signals processing in the transmission chain (6), the total number of elementary modules or sets of elementary modules (6_1, 6_2,...,6_n) for the signals processing of such transmission chain (6) being in this way higher than the number of sub-machines of said plurality of sub-machines (SMi), in such a way as to be able to face at the same time several situations of malfunction or failure of the same modules.

10. Architecture for the management of transmission channels according to any one of the claims from 3 to

9, characterised in that each elementary module comprises an input controller (14) connected to an output controller (15) amongst which there is a first memory bank (16) and a second memory bank (17), operating alternatively between each other for carrying out a substitution of information in the main channel of serial transmission(10), this way of operation being of the generic so-called "ping-pong" type.

11. Architecture for the management of transmission channels according to claim 10, characterised in that both the serial transmission channel (10) and the serial transmission channel of redundancy (11) can carry a sequence of informative units however organised, even varying compared to reconfigurations of the switch, remote controlled in order to be able to face possible failures, by presenting only a time consistence in the sequence of information received, said time consistence being deterministic, that is, definitely reconstructable based on suitable indices at the end of each transmission chain (6, 7).

12. Architecture for the management of transmission channels according to claim 11, characterised in that the main serial transmission channel (10) transmits numeric information subdivided into a plurality of groups (informative units FU) in turn comprising a plurality of bits organised according to the time, and in that each module of a transmission chain (6, 7) extracts a set of information from the main serial transmission channel (10) and gives it back to said channel after having re-elaborated it in such a way as to shift it temporally or to move it from one of said blocks (informative units, FU) to another.

13. Architecture for the management of transmission channels according to claims 4 and 7, characterised in that said input demultiplexers (8, 12) and said output multiplexers (9, 13) act on a single bit, thus minimising the number of registers necessary for carrying out such operations and also therefore the power consumption.

14. Architecture for the management of transmission channels according to claim 1, characterised in that it comprises groups of machines designed on the same physical support and connected between each other by means of a passive bus structure, each sub-machine of said groups operating on groups of bit not temporally adjacent.

15. Structure for the transmission and channelling of digital signals connected to at least one input channel and at least one output channel, characterised in that it comprises at least one chain (6) of elementary modules or set of elementary modules (6_1, 6_2,...,6_n) for the signals processing connected in cascade between each other by means of a main serial transmission channel of the pipeline type (10), each elementary module or set of elementary modules (6_1, 6_2,...,6_n) taking in input from the main serial transmission channel (10) its own binary information pertaining thereto and feeding in output to the main serial transmission channel (10) binary information which is already processed, regenerating at the same time the information carried by the main serial transmission channel (10) itself before feeding it to the next elementary module, so regenerating the entire main serial transmission channel (10) passing from one elementary module to the other.

16. Structure for the transmission and channelling of digital signals according to claim 15, characterised in that elementary modules or sets of elementary modules (6_1, 6_2,...,6_n) for the signals processing are further connected in cascade between each other by means of a serial transmission channel of redundancy (11), in such a way as to be able to face situations of malfunction or failure of the main serial transmission channel (10).

17. Structure for the transmission and channelling of digital signals according to claim 16, characterised in that it comprises a second chain (7) of elementary modules or sets of elementary modules (7_1, 7_2,...,7_n) for the signals processing connected in cascade between each other by means of said main serial transmission channel (10) and said serial transmission channel of redundancy (11).

18. Structure for the transmission and channelling of digital signals according to claim 15, characterised in that each elementary module comprises an input controller (14) connected to an output controller (15) between which there is a first memory bank (16) and a second memory bank (17), operating alternatively between each other for carrying out a substitution of information in the main serial transmission channel (10), with a way of operation of the generically so-called "ping-pong" type.

19. Structure for the transmission and channelling of digital signals according to claim 15, characterised in that both the main serial transmission channel (10) and the serial transmission channel of redundancy (11) can carry a sequence of informative units however

organised, even varying in response to reconfigurations of the switch, remote controlled in order to be able to face possible failures, presenting only a time consistence in the sequence of information received, said time consistence being deterministic, that is, definitely reconstructable, based on suitable indices at the end of each transmission chain (6, 7).

20. Structure for the transmission and channelling of digital signals according to claim 19, characterised in that the main serial transmission channel (10) transmits digital information subdivided into a plurality of groups (informative units, FU) each one comprising a plurality of bits organised according to the time, and in that each module of a transmission chain (6, 7) extracts a set of information from the main serial transmission channel (10) and gives it back to said channel after having re-elaborated it in such a way as to shift it temporally or to move it from one of the said blocks (informative units, FU) to another.

21. Structure for the transmission and channelling of digital signals according to claim 16, characterised in that it comprises a plurality of input channels and a plurality of output channels connected to said main serial transmission channel (10) respectively by means of an input demultiplexer (8) and an output multiplexer (9) and to said serial transmission channel of redundancy (11) respectively by means of an input demultiplexer of redundancy (12) and an output multiplexer of redundancy (13).

22. Architecture for the management of transmission channels according to claim 5, characterised in that several sub-machines or elementary modules, comprise

sub-machines at a lower level, connected between each other via a passive bus with interlacing operation.

23. Architecture for the management of transmission channels according to claim 22, characterised in that it comprises spare sub-machines connected to the passive bus, in order to be able to face possible failures via remote control, thus increasing the reliability of the single elementary modules connected to the serial bus.

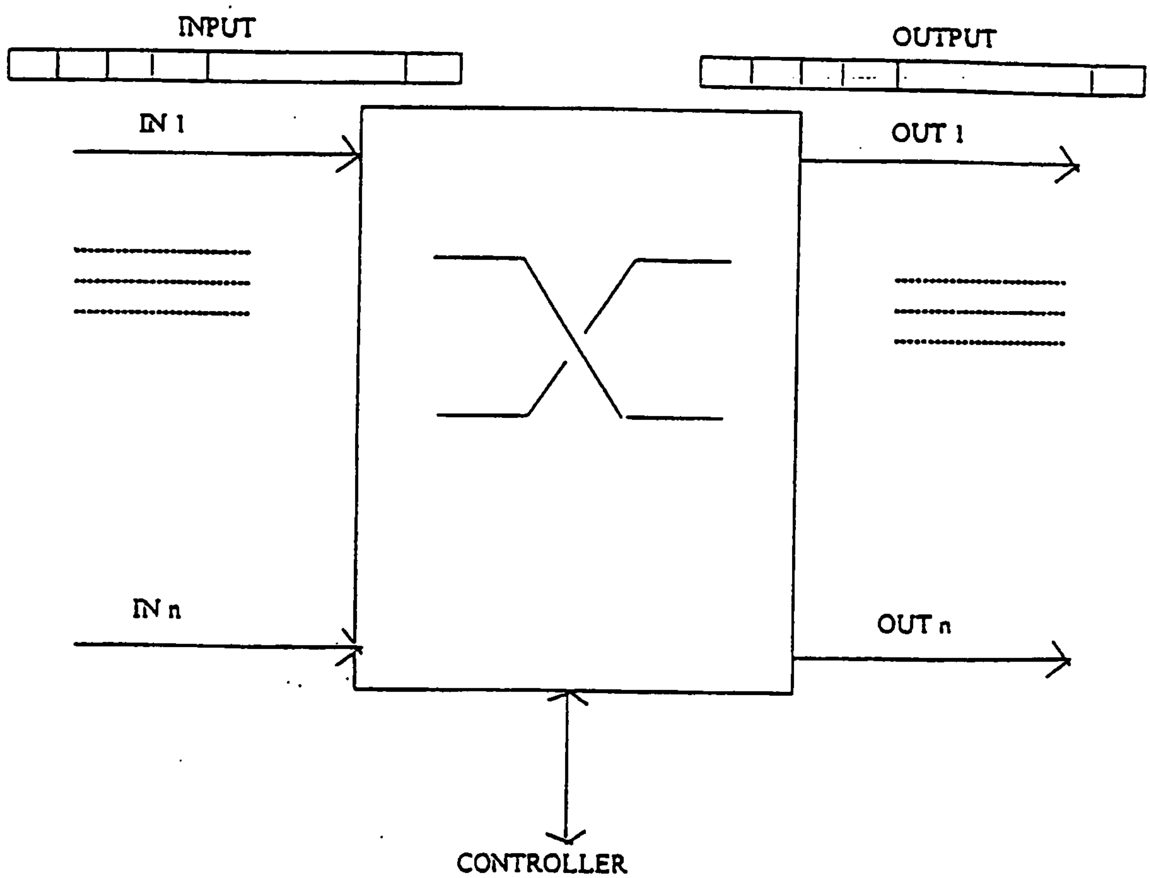


FIG. 1A

2/5

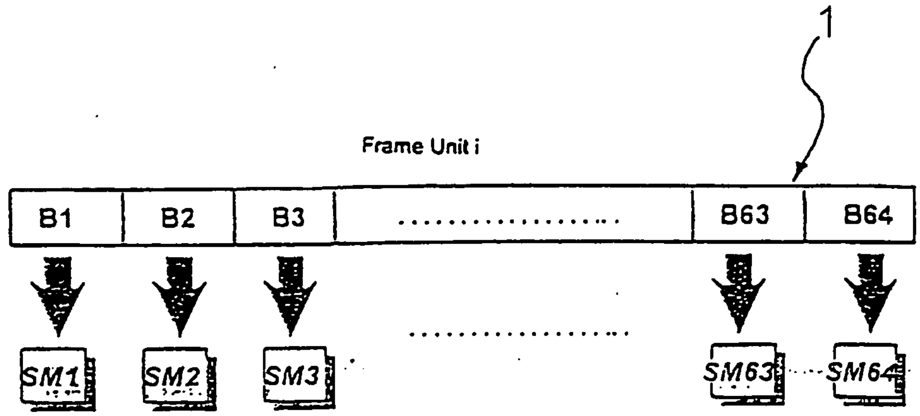


FIG. 1B

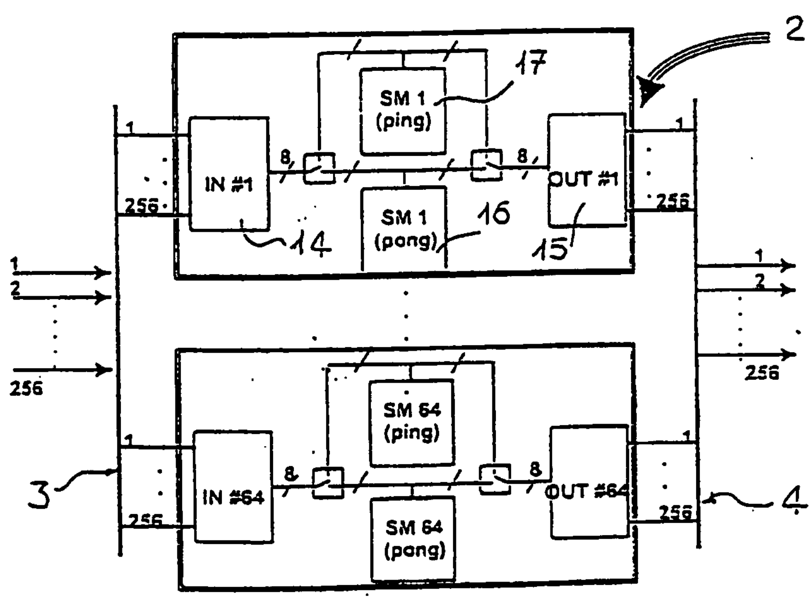


FIG. 2

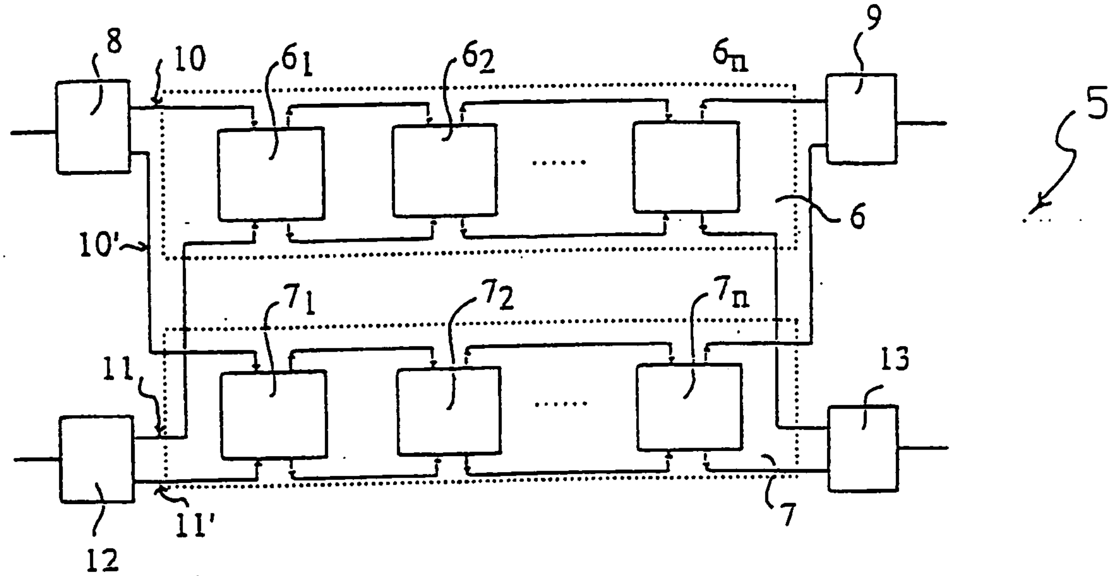

8
10
6_1
6_2
6_n
9
5
6
10'
7_1
7_2
7_n
11
13
12
11'
7

FIG. 3

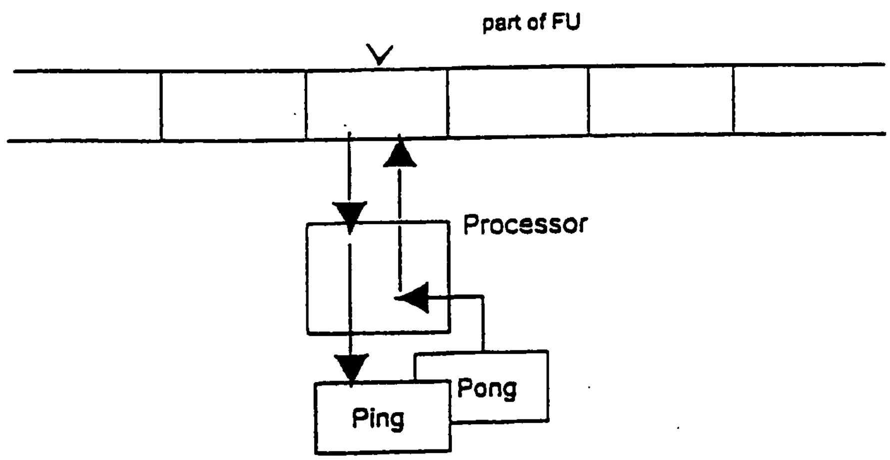
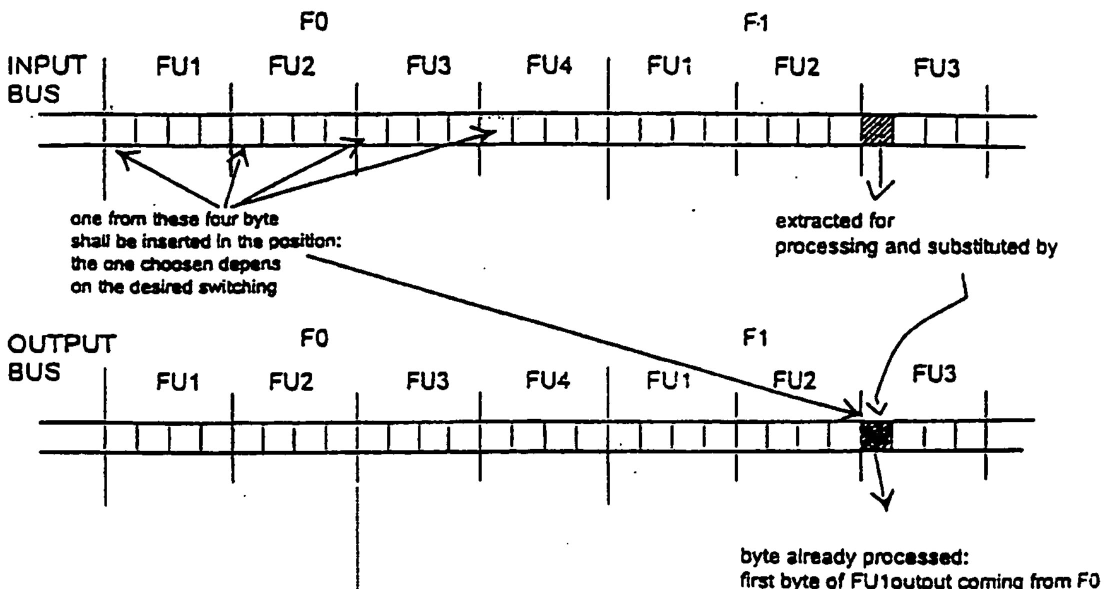

part of FU
Processor
Pong
Ping

FIG. 4

FIG. 5


F0
F1
INPUT BUS
FU1
FU2
FU3
FU4
FU1
FU2
FU3
one from these four byte
shall be inserted in the position:
the one choosen depens
on the desired switching
extracted for
processing and substituted by
OUTPUT BUS
F0
F1
FU1
FU2
FU3
FU4
FU1
FU2
FU3
byte already processed:
first byte of FU1output coming from F0

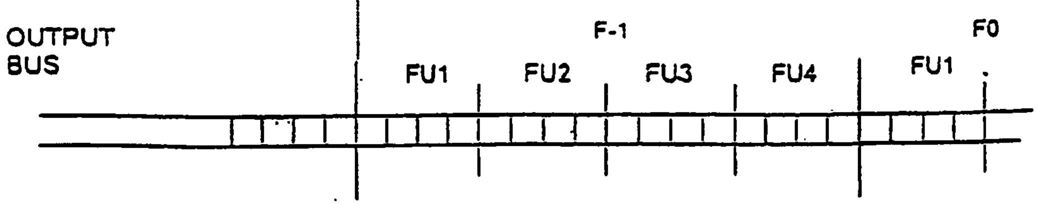

OUTPUT BUS
F-1
F0
FU1
FU2
FU3
FU4
FU1

FIG. 6

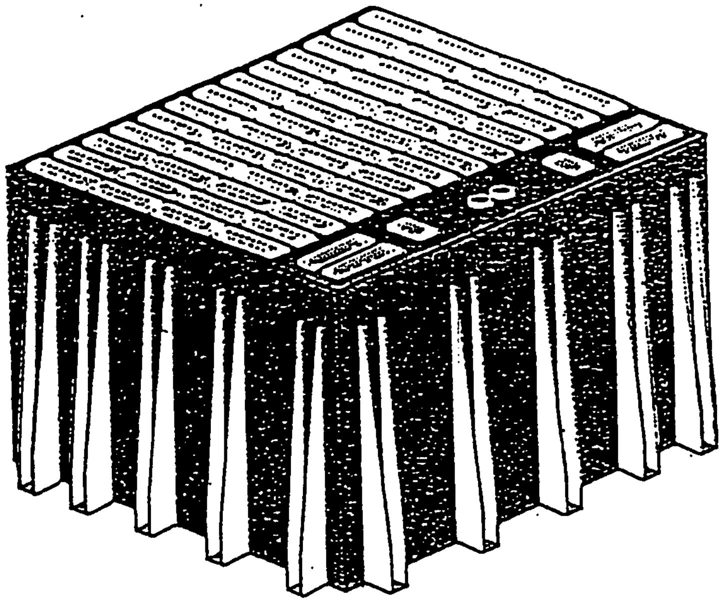


FIG. 7

INTERNATIONAL SEARCH REPORT

International Application No
PCT/IT 98/00284

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04Q11/04 H04B7/204

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04Q H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 220 320 A (ASSAL F T ET AL) 15 June 1993 see abstract see column 4, line 61 - column 5, line 24 see column 9, line 31 - column 10, line 31 see claim 1; figures 1,2,4,8-10; table 1	1-9, 15-17,21
Y		14,22,23
A		10,13,18

Y	FR 2 596 606 A (LMT RADIO PROFESSIONELLE) 2 October 1987 see abstract see page 4, line 11 - page 5, line 24 see figures 3,4	14,22,23

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
5 July 1999	19/07/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Gijsels, W

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INTERNATIONAL SEARCH REPORT

Int. ...tional Application No
PCT/IT 98/00284

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 696 470 A (GUPTA R K ET AL) 9 December 1997 see abstract see column 1, line 25-49 see column 3, line 55-64 see column 4, line 26-39 see figures 1A,1B,4,5A-D	1-3,6,8, 9
A		5,10, 13-18,23

X	BERNER W ET AL: "MOBS - A MODULAR ON-BOARD SWITCHING SYSTEM" IEEE GLOBAL TELECOMMUNICATIONS CONFERENCE & EXHIBITION, vol. 3 of 3, 28 November 1988 - 1 December 1988, pages 1769-1773, XP000043798 HOLLYWOOD, FLORIDA see the whole document	1,3,4, 6-8
A		5,15-17, 21

X	DE 37 35 853 C (ANT NACHRICHTENTECHNIK GMBH) 11 May 1989 see abstract see column 2, line 7-10 see column 3, line 42 - column 4, line 31 see figures 1,3A-C	1,3,4, 6-8
A		5,15-17, 21

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/IT 98/00284

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FR 2596606 A	02-10-1987	NONE	
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DE 3735853 C	11-05-1989	NONE	